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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/622,287	07/18/2003	Rahul Saxena	42P16855	4600

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EXAMINER	
HUSSAIN, TAUQIR	
ART UNIT	**PAPER NUMBER**
2152	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/29/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/622,287	SAXENA, RAHUL	
	Examiner	Art Unit	
	Tauqir Hussain	2152	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-27 are pending in this application.

Information Disclosure Statement

2. The listing of references in the specification is not a proper information disclosure statement. 37 CFR 1.98(b) requires a list of all patents, publications, or other information submitted for consideration by the Office, and MPEP § 609.04(a) states, "the list may not be incorporated into the specification but must be submitted in a separate paper." Therefore, unless the references have been cited by the examiner on form PTO-892, they have not been considered.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claim 1-27 are rejected under 35 U.S.C. 102(b) as being anticipated by Viswanath et al. (Patent Number: 6151322), hereinafter "Viswanath".

5. As to claim 1, Viswanath discloses, a method of operating a network device, comprising:

receiving electronic data from a first port of the data networking device (Abstract, lines 1-2);

deleting at least a portion of the electronic data prior to providing the electronic data to the memory of the networking device Abstract, lines 3-10, where striping the tag means deleting the portion of the electronic data);

providing at least a portion of the electronic data to a second port (Abstract, lines 16-20, where transmitting port is the second port).

6. As to claim 10, an apparatus, comprising:

one or more receive ports capable of receiving electronic data from a network (Col.7, liens 10-11, where switch receiving packets on one of the ports);

one or more transmit ports capable of transmitting electronic data to a network (Col.7, lines 42-44);

a memory (Col.7, lines 12-13; and

a processor, the processor configured to, in operation (Fig.3, Element-70):

delete at least a portion of the electronic data received by the one or more receive ports (Col.7, line 12, where extracted means deleting the header from the data frame/packet);

provide the remaining electronic data to the memory (Col.7, line 13);

read the electronic data from the memory (Col.7, lines 17-18);

modify the electronic data after reading from the memory (Col.7, lines 32-33); and

provide at least a portion of the electronic data to one or more of the transmit ports (Col.7, lines 42-44).

7. Claim 19, is rejected for the same reasons applied above to claims 1 and 10.

8. As to claim 2, Viswanath discloses, modifying the electronic data prior to said providing Abstract, lines 3-5, where striping is modifying).

9. As to claim 3, Viswanath discloses, wherein the electronic data comprise a frame (Col.1, lines 19-22).

10. As to claim 4, Viswanath discloses, wherein the portion of electronic data deleted comprises a VLAN (virtual local area network) tag (Abstract, line 3).

11. As to claim 5, Viswanath discloses, wherein modifying comprises inserting a VLAN tag to the frame (Abstract, lines 14-16).

12. As to claim 6, Viswanath discloses, generating a CRC (cyclic redundancy code) and inserting the CRC into the frame prior to providing to the memory (Fig.4, Elements-84 and 64, Col.7, lines 21-39, where comparator is CRC and modifying means adding or deleting or inserting the appropriate information into frame and sending it to memory 64).

13. As to claim 7, Viswanath discloses, providing a portion of the electronic data to a control module prior to deleting a portion of the electronic data (Fig.4, Elements-84 and 64, Col.7, lines 17-21, where comparator 84 is control module, lines 32-33, where data is modified means deleting or adding header information and lines 37-39, where data is transferred to element-64, which is memory).

14. As to claim 8, Viswanath discloses, wherein the portion of data provided to the control module comprises the protocol header (Fig.1a and 1b, Col.3, lines 31-33, Inherently protocol header is there, e.g. VLAN type, source address, destination address etc.).

15. As to claim 9, Viswanath discloses, wherein the first port and the second port comprise a receive port and a transmit port, respectively (Col.7, lines 10, where receiving port could be first port and lines 42-44, where output port is transmit port).

16. As to claim 11, Viswanath discloses, wherein the processor is further configured to modify the electronic data prior to providing at least a portion of the electronic data to one or more of the transmit ports (Col.7, lines 42-44, where out put port is transmit port and VLAN insertion means the data has been modified).

17. As to claim 12, Viswanath discloses, wherein the apparatus comprises a network switch (Fig.2, Col.7, lines 10-11, where network switch means apparatus).

18. As to claim 13, Viswanath discloses, wherein said memory comprises network switch internal memory (Fig.4, Element-64 and 80).

19. As to claim 14, is rejected for the same reasons applied above to claim 4.

20. As to claim 15, Viswanath discloses, wherein modifying the electronic data comprises inserting a VLAN tag, wherein the VLAN tag relates at least in part to the destination address of the electronic data (Col.7, lines 42-44, where VLAN tag is inserted as a destination address).

21. As to claim 16, Viswanath discloses, wherein the processor comprises a network processor (Fig.3b, Element-70, Col.6, lines 25-26, where network switch has decision making engine which is processor and since switch is a network device therefore, processor is a network processor).

22. As to claim 17, Viswanath discloses, wherein the memory comprises a plurality of memory devices (Fig.3b, Elements-32, 64 and 66; Col.5, lines 50-51 and 56).

23. As to claim 18, Viswanath discloses, wherein the plurality of memory devices comprise one or more of:

random access memory (Col.7, line 62) and

synchronous dynamic random access memory (Col.5, lines 7-9).

24. Claims 20-26 are rejected for the same reasons as applied above to claims 5, 4, 6 and 15-18 respectively.

25. As to claim 27, the system of claim 19, wherein said processor is configured to modify said electronic data only if said second port is configured to recognize tags (Col.7, lines 10-13, where processor processes the tagged packets and lines 42-45, transmitted to VLAN ports which means there are out put ports configured to handle tagged packets).

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tauqir Hussain whose telephone number is 571-272-1247. The examiner can normally be reached on 7:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bunjob Jaroenchonwanit can be reached on 571 272 3913. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TH

BUNJOB JAROENCHONWANIT
SUPERVISORY PATENT EXAMINER